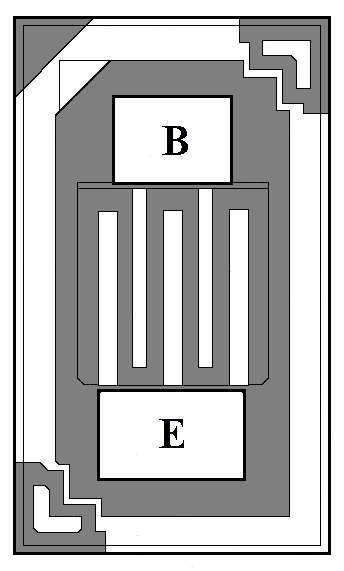
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.012”**



**.0032 x .0048**

**.0032 x .0038**

**.019”**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: B = .0032” X .0038” E = .0032” X .0048”**

**Backside Potential: Collector**

**Mask Ref: SMN**

**APPROVED BY: DK DIE SIZE .012” X .019” DATE: 9/29/22**

**MFG: SPRAGUE/ALLEGRO THICKNESS .008” P/N: 2N3906**

**DG 10.1.2**

#### Rev B, 7/19/02